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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,571	10/31/2003	Kenneth Dockser	RPS920030151US1	1590

45503 7590 10/29/2008

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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
10/29/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,571	DOCKSER, KENNETH	
	Examiner	Art Unit	
	BRIAN P. JOHNSON	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2008*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,7-10 and 21-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4, 7-10, and 21-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 4, 7-10, and 21-34 are pending.

Papers Filed

2. Examiner acknowledges receipt of remarks and amendments filed on 24 July 2008.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 4, 7-9, 21-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (U.S. Patent No. 5,187,796) in view of Matsuo (U.S. Patent No. 5,901,301) in further view of Sih (U.S. Patent No. 6,557,022)

4. As per claim 1, Wang discloses a microprocessor, comprising:

a vector unit (Fig. 3 ALUs 46, 48 and 50) to execute a vector instruction to perform a first operation on a first set of data operands and a second operation on a second set of operands. *The examiner asserts that the processor performs a multiply*

followed by an operand rotate right for the FMULR instruction listed in the col. 27 table. Both operations (multiply and rotate) operate on both sets of operands.

Wherein the vector instruction includes a first register field indicative of a first primary register in the primary register file and a first secondary register in the secondary register file, a second register field indicative of a second primary register in the primary register file and a second secondary register in the secondary register file, and a third register field indicative of a third primary register in the primary register file and a third secondary register in the secondary register file; and

Wherein the first set of operands includes a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register (Fig. 3 register files 40 and 42, col 27 lines 22-24 and col 27 table). *The examiner asserts that complex pairs of real and imaginary numbers are simply alternate labels for two-dimensional vector data. The data stored in register file 40 corresponds to an "x" vector, and constitutes a real portion of a number and the data stored in register file 42 corresponds to a "y" vector and constitutes an imaginary number. This is considered to be the "primary" and "secondary" register file as claimed. See col 8 lines 47-53.*

Wang fails to disclose 3-input execution units.

Matsuo discloses wherein a 3-input primary floating point unit is configured to multiply first and third operands and further configured to add the second operand to or subtract the second operand from the resulting product. (Col. 27 lines 47-52)

Matsuo discloses his invention to promote "high-speed digital signal processing" by taking advantage of "processing frequently used in signal processing such as a multiply-add operation at high speeds." (Matsuo col. 1 lines 13-16) Wang discloses "DSPs were developed to exploit the successive multiply/accumulate nature of signal processing." (Wang col. 3 lines 24-26) Matsuo's desired outcome of higher processing speeds through optimizing common instructions coincides with that of Wang.

It would have been obvious to one of ordinary skill in the art at the time of invention to have included Matsuo's method of adding a third operand to the product of first and second operands in Wang's invention for the benefit of higher speed processing. The combination would logically require that each of the i, j, and k portions to have separate execution units (as shown in Wang fig 4) that include three inputs that complete a separate multiply-accumulate for each dimension.

Wang/Matsuo fails to clearly disclose whether the inputs to the MAC unit are received at substantially the same time.

Sih discloses a MAC unit that contains enough output ports to the register file to allow the MAC unit to receive all its inputs at the same time (fig. 2; col 3 lines 13-30).

Wang/Matsuo would have been motivation to utilize this technique in order to simplify the MAC inputs and allow enough output ports to feed as many execution units as necessary without waiting additional clock cycles.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Wang/Matsuo and incorporate the timing

requirement of Sih that allows all inputs to the MAC unit to be received at substantially the same time.

5. As per claim 4, Wang/Matsuo/Sih discloses the microprocessor of claim 3, wherein the vector unit includes a primary floating point unit (Fig. 3 FPU 46) and a secondary floating point unit (Fig. 3 FPU 48), wherein the primary floating point unit is configured to perform a floating point operation on the first set of operands and the secondary floating point unit is configured to perform a floating point operation on the second set of operands. The addition of Matsuo discloses 3-input execution units. *Col. 27 table lists instructions as "floating point operations", hence, the FPUs are configured to perform floating point operations.*

6. As per claim 7, Wang/Matsuo/Sih discloses the microprocessor of claim 2, wherein the vector unit is further characterized as being enabled to perform a cross instruction in which the first and second operations both use at least one operand from the primary register file and at least one operand from the secondary register file. (Col. 26 lines 22-45)

7. As per claim 8, Wang/Matsuo/Sih discloses the microprocessor of claim 2, wherein the vector unit is further characterized as being enabled to perform a cross-replicate vector instruction in which the first and second operations are both performed using at least one common operand. *The examiner asserts that the FMULR operation*

performs a multiply, and then a component rotate using the same operands as the multiply.

8. As per claim 9, Wang/Matsuo/Sih discloses the microprocessor of claim 2, wherein the vector unit is configured to store a real portion of a complex number in the primary register file and an imaginary portion of the complex number in the secondary register file. *The examiner asserts that complex pairs of real and imaginary numbers are simply alternate labels for two-dimensional vector data. The data stored in register file 40 corresponds to an "x" vector, and constitutes a real portion of a number and the data stored in register file 42 corresponds to a "y" vector and constitutes an imaginary number.*

1. Regarding claim 21, Wang/Matsuo/Sih discloses the microprocessor of claim 1, wherein the second set of operands include a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register (col 8 lines 53-59).

2. Regarding claim 22, Wang/Matsuo/Sih discloses the microprocessor of claim 4 wherein the first operation includes multiplying two of the three first set of operands to obtain a first product and adding or subtracting the remaining of the first set of operands to or from the first product and wherein the second operation includes multiplying two of

the three second set of operands to obtain a second product and adding or subtracting the remaining of the second set of operands to or from the second product (Matsuo (col 27 lines 47-52)

3. Regarding claim 23, Wang/Matsuo/Sih discloses the microprocessor of claim 22, wherein the first and second sets of operands comprise first and second set of floating point formatted operands (col 27 table—note "floating-point operations").

4. Regarding claim 24, Wang/Matsuo/Sih discloses the microprocessor of claim 1, wherein the vector register file wherein the vector instruction includes a target register field indicative of a primary target register in the primary register file and a secondary target register in the secondary register file (fig. 14 and col 24 lines 49-51) and further wherein the vector unit is further configured to store a result of the first operation in the primary target register and to store a result of the second operation in the secondary target register. *Examiner asserts that vector registers 40 and 42 can store the result of the first and second operands.*

5. Regarding claim 25, Wang/Matsuo/Sih discloses a vector trait to process a vector instruction having an opcode and first, second, and third register fields (col 27 table), comprising: a register file including a primary register file having a set of primary registers (fig 3 reference 40) and a secondary register file having a set of secondary registers (fig. 3 reference 42), wherein the register field identifies a register in the

primary register file and a corresponding register in the secondary register file (col 8 lines 48-53— "i" and "j" portions); primary and secondary calculating units (fig. 4 reference 46 and 48), wherein the primary calculating unit includes first, second, and third inputs to receive, respectively, first, second, and third operands of a first set of operands and wherein the secondary calculating unit includes fast, second, and third inputs to receive, respectively, first, second, and third operands of a second set of operands (Matsuo Col. 27 lines 47-52) and multiplexing circuitry controlled by the opcode to select each of the first, second, and third operands in the first and second set of operands from the set of primary and secondary file registers identified by the register fields. *Examiner asserts that multiplexing circuitry inherently exists because different inputs are required to enter the execution units for different calculations.*

6. Regarding claim 26, Wang/Matsuo/Sih discloses the vector unit of claim 25, wherein the multiplexing circuitry is controlled by the opcode to select: the first operand in the first set of operands from either the first primary or the first secondary registers (col 27 table—*Examiner asserts that the opcode controls the register value that enters the execution unit; therefore, it control the multiplexing circuitry*); the second operand in the first set of operands from either the second primary or the second secondary registers (col 8 lines 53-59); and the third operand in the first set of operands from either the third primary or the third secondary registers (col 8 lines 53-59); the first operand in the second set of operands from either the first primary or the first secondary registers, the second operand in the second set of operands from either the second primary or the

second secondary registers; and the third operand in the second set of operands from either the third primary or the third secondary registers (col 8 lines 53-59 and col 27 table).

7. Regarding claim 27, Wang/Matsuo/Sih discloses the vector unit of claim 25, wherein the primary calculating unit is controlled by the opcode to perform a first operation on the first set of operands and the secondary calculating unit is controlled by the opcode to perform a second operation on the second set of operands (Matsuo Col. 27 lines 47-52—*Examiner asserts that the MAC opcode would control the execution units of both primary and secondary portions*).

8. Regarding claim 28, Wang/Matsuo/Sih discloses the vector unit of claim 27, wherein the first operation differs from the second operation.

Examiner asserts that the operations are completed on two different sets of operands, therefore, the two operations differ.

9. Regarding claim 29, Wang/Matsuo/Sih discloses the vector unit of claim 27, wherein the first and second operations both include multiplying their respective first and third operands to obtain respective first products and adding or subtracting their respective second operands to or from the respective first products (Matsuo Col. 27 lines 47-52).

10. Regarding claim 30, Wang/Matsuo/Sih discloses the vector unit of claim 25, wherein the first, second, and third operands of the first and second sets of operands are all floating point formatted operands (col 27 table).

11. Regarding claim 31, Wang/Matsuo/Sih discloses a microprocessor including: an execution unit enabled to execute an asymmetric instruction, wherein the asymmetric instruction includes a set of three operand register fields and a target register field and an operation code (opcode) (col 24 lines 49-51); a register file accessible by the execution unit and having a rank of two including a primary register file (fig 3 reference 40) and a secondary register file (fig 3 reference 42) wherein a value in an operand register field identifies a register in the primary register file and a corresponding register in the secondary register file (col 8 lines 53-59); wherein the execution unit is configured to perform a first operation on a first set of three operands (Matsuo Col. 27 lines 47-52) selected from registers identified by the set of operand register fields and to perform a second operation on a second set of three operands also selected from the registers identified by the set of operand registers fields (see combination) wherein the first and second operations and. selection of the first and second sets of operands are determined by the opcode.

Examiner asserts that the opcode determines that the operands are of type multiply-accumulate.

12. Regarding claim 32, Wang/Matsuo/Sih discloses the microprocessor of claim 31, where at least one condition selected from the group of conditions consisting of the first and second operations being different and the first and second sets of operands being different is true.

Examiner asserts that the operands are different (i.e. one includes the "i" operands and the other includes "j" operands). Consequently, the operations are considered to be different.

13. Regarding claim 33, Wang/Matsuo/Sih discloses the microprocessor of claim 31, wherein the execution unit is further configured to store a result of the first operation in a register of the primary register file determined by the target register field and the result of the second operation in a register of the secondary register field also determined by the target register field (Matsuo Col. 27 lines 47-52).

14. Regarding claim 34, Wang/Matsuo/Sih discloses he microprocessor of claim 31, including multiplexing circuitry controlled by the opcode to select a first of the first set of three operands from a first primary and a first secondary register identified by a first operand register field, a second of the first set of three operands from a second primary and a second secondary register identified by a second operand register field, a third of the first set of three operands from a third primary and a third secondary register identified by a first operand register field (col 8 lines 53-59) , a first of the second set of three operands from a first primary and a first secondary register

identified by a first operand register field, a second of the second set of three operands from a second primary and a second secondary register identified by a second operand register field, and a third of the second set of three operands from a third primary and a third secondary register identified by a first operand register field (col 27 table).

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang/Matsuo/Sih in view of Golliver et al. (U.S. Publication No. US 2002/0004809) hereinafter referred to as Golliver.

10. As per claim 10, Wang/Matuo discloses the microprocessor of claim 9, but fails to disclose wherein the vector unit is configured to perform a complex operation in which the imaginary portion of a first operand is multiplied by an imaginary portion of a second operand in the first operation and in which the imaginary portion of the first operand is multiplied by a real portion of the second operand in the second operation.

11. Golliver discloses a vector unit configured to perform a complex operation in which the imaginary portion of a first operand is multiplied by an imaginary portion of a second operand in the first operation (AiBi in Fig. 3A) and in which the imaginary portion of the first operand is multiplied by a real portion of the second operand in the second operation (AiBr in Fig. 3A).

12. Golliver discloses “a data manipulation instruction for enhancing value and efficiency of performing complex arithmetic instructions.” (Paragraph 2) Golliver’s desired outcome coincides with that of Wang: increased efficiency of processing.

13. It would have been obvious to one of ordinary skill in the art at the time of invention to have included Gollivers method of complex number arithmetic in Wang's processor for the benefit of increased processing efficiency.

Response to Arguments

15. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

16. To clarify the record, on pages 8-9 of Applicant's remarks, the following is stated:

> *Applicants' claims now clarify and/or more clearly recite that the vector unit has three inputs and receives three operands at the same time. The failure of the reference to teach or suggest these features is clearly established by Examiner within the Examiner's Response section of the Office Action. Given that Examiner has already admitted to these shortcomings within the reference, the present claim amendments necessarily overcome the present rejection.*

This statement is completely false. In the Office Action mailed 11 June 2008 Examiner stated:

> *Applicant argues that the multiply-accumulate function does not proved three operands to the execution unit "at the same time" or "simultaneously." **Examiner does not concede this [point]**, but respectfully notes that this limitation is in no way required by the claim. (emphasis added)*

Examiner expressly and clearly stated that there was no admission to the timing requirement in the last action. Examiner respectfully requests that Applicant take care not to misquote the record on such an important point.

That being said, now that a time timing requirement is required by the claims, Examiner notes that the references on record do not clearly show the point at which all operands are received. For that reason, an additional reference has been added that more clearly shows the timing of operands within a multiply-accumulate unit.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Seshan (U.S. Patent No. 6,061,787) discloses a processor consisting of multiple parallel register files.

Tromp et al. (U.S. Publication No. US 2005/0283592) disclose a system executing two operations based on a single instruction.

Gochman et al. (U.S. Patent No. 6,920,546) disclose a system with multiple operations in an instruction word sharing common operands.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183